High Performance VLSI Design Using Body Biasing in Domino Logic Circuits

Suman Nehra[1], K.G.Sharma[2], Tripti Sharma[3] and Prof.B.P.Singh[4]

[1]*Deptt. of Electronics and Communication Engg., FET-MITS Lakshmangarh, Rajasthan (INDIA)*
[2]*Suresh Gyan Vihar University, Jagatpura, Jaipur, Rajasthan (India)*
E-mail: [1]nehra.sumanvlsi@gmail.com, [2]sharma.kg@gmail.com,[3] tripsha@gmail.com,[4] bpsingh@ieee.org

***Abstract*— Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power Consumption. Dynamic CMOS circuits, featuring a high speed operation are used in high performance VLSI designs. In this work, domino AND gate is designed with various body biasing and high performance circuit was specified. The proposed design is tested in 65nm and 45nmto prove its technology independence.**

***Index Terms* - CMOS, Conventional body bias, Domino logic, Dynamic power, Substrate Biasing.**

I. INTRODUCTION

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]. The power consumed in high performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality [2]-[3]. If the current trend in increasing power continues, high performance microprocessor will soon consume thousands of watts. The power density of a high performance microprocessor will exceed the power density levels encountered in typical rocket nozzles within the next decade [4]. Domino logic circuits, however, are highly sensitive to noise as compared to static gates. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[5]. The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems. Dynamic switching power, the dominant component of the total power consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, degrades circuit speed due to reduced transistor currents.

Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1] – [4]. At reduced threshold voltages, however, sub threshold leakage currents increase exponentially. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits. However, deep sub micrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge.

Over the past decade, considerable research is devoted to the development of energy-efficient VLSI circuit and systems for portable systems [9] – [11]. To achieve portability, the system must have a miniaturized power supply. A portable system must be designed for low power consumption. An effective way to reduce power consumption is supply voltage scaling. However, threshold voltage cannot be scaled down with the same rate. Thus for low power applications, sub-threshold operation is a better option. Low power systems are slower ones, because of trade-off between power and speed. Thus the repeater circuit operating in sub-threshold region at medium frequencies is a better option. The sub threshold logic operates with the power supply V_{dd} less than the threshold voltage V_{th} of the transistor.

In this paper domino AND gates with different substrate biasing techniques and Conventional Body Bias inverter are designed and their performances are compared. Power consumption, delay are used as parameters at different frequencies, supply voltages and temperatures in sub threshold region. The designs are tested and compared at 65 nm and 45 nm technologies to prove the technology independence of the proposed design The rest of the paper is organized as follows: In Section II various Circuit techniques in domino logic circuits for power reduction and delay reduction are proposed. In Section III simulation and implementation

results are presented. Finally, conclusions are presented in Section V.

II. CIRCUIT TECHNIQUES

Dynamic domino logic circuits are widely used in modern VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power Consumption. This work discusses several domino circuits design techniques to reduce the power Consumption of domino logic while simultaneously improving noise immunity. Domino logic gates are frequently employed in high performance circuits for high speed and area efficiency. As supply voltage is reduced, delay increases, unless threshold voltage V_T is also decreased. Substrate biasing provides an effective circuit-level technique for varying threshold voltage, as can be seen in (1) below.

$$V_T = V_{TO} + \gamma\left(\sqrt{|V_{SB} - 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right)$$

Here V_{TO} is the zero-bias threshold voltage, γ the body-effect coefficient, V_{SB} the source-to-bulk voltage, Φ_F the quasi-Fermi potential.

For different biasing schemes, the output inverter is zero body biased figure 1.

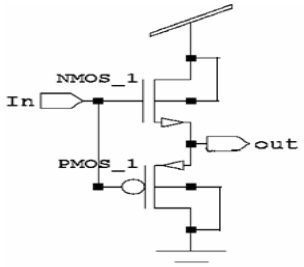

Fig. 1 conventional body-biasing inverter

Different biasing schemes are shown below:-

In order to enhance the performance of the circuit, various body biasing techniques are used.

The substrate of the MOS transistors is connected in six different ways. Six body biasing schemes for the evaluation networks are shown in figure 2.

1. The substrate of NMOS is connected to clock and the substrate of PMOS is connected to supply voltage V_{DD} (SB1).
2. The substrate of NMOS and PMOS is connected to clock (SB2).
3. The substrate of NMOS is connected to supply voltage V_{DD} and the substrate of PMOS is connected to clock (SB3).
4. The substrate of NMOS is connected to supply voltage V_{DD} and the substrate of PMOS is connected to Ground (SB4).
5. The substrate of NMOS and PMOS both connected to supply voltage V_{DD} (SB5).
6. The substrate of NMOS is connected to its source terminal and the substrate of PMOS is connected to clock (SB6).

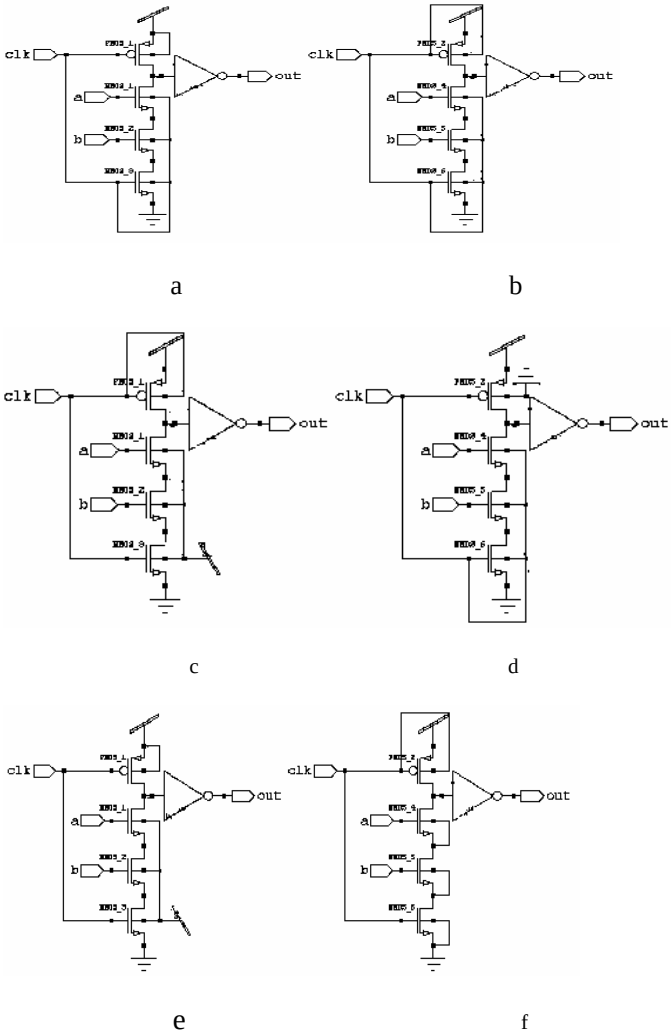

Fig. 2.(a)SB1,(b)SB2, (c)SB3, (d)SB4, (e)SB5, (f)SB6

Minimum energy in sub threshold region then depends not only on supply voltage but also on the sub threshold bias voltage.

III. SIMULATION AND IMPLEMENTATION RESULTS

The designs are simulated using 45nm and 65nm technology. Designs are tested in different biasing conditions where different voltages, operating frequencies, and temperatures are taken.

Supply voltage, frequency and temperature are taken as parameters. The standard temperature value of 25°C, input signal frequency of 500 kHz, and supply voltage of 0.22 V in 45 nm and 0.36 V in 65 nm are used. Power consumption, delay are measured keeping one parameter variable with two other parameters constant, e.g. , power consumption is calculated at various

.

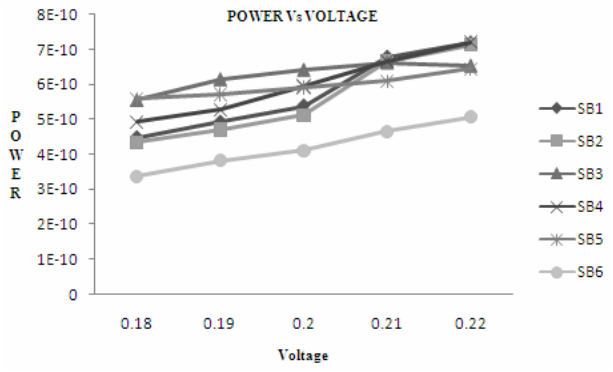

Fig. 3 Power Consumption at different voltages in 45 nm technology

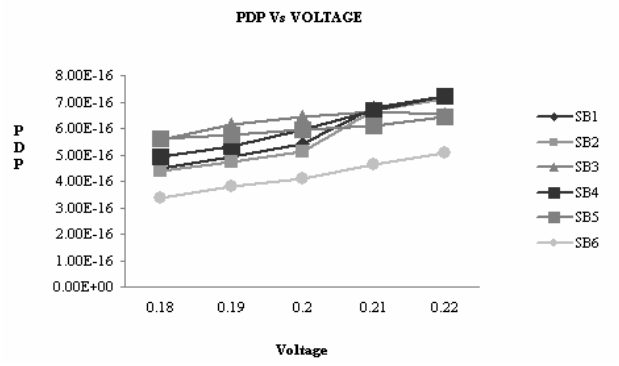

Fig. 4 Power-Delay Product at various voltages in 45 nm technology

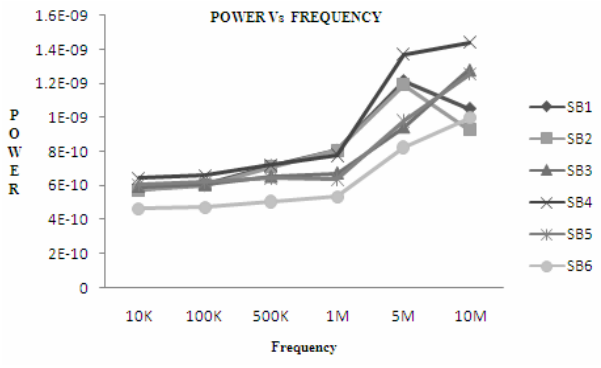

Fig. 5 Power Consumption at different frequencies in 45 nm technology

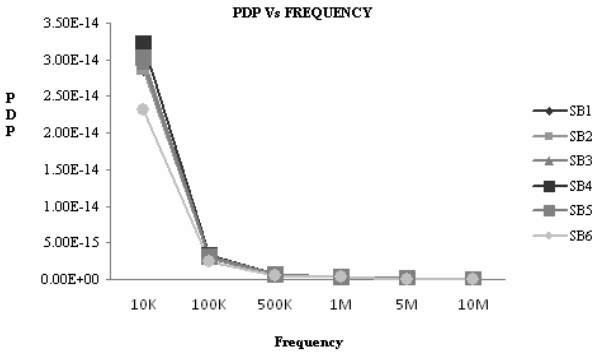

Fig. 6 Power-Delay Product Vs frequency in 45 nm technology

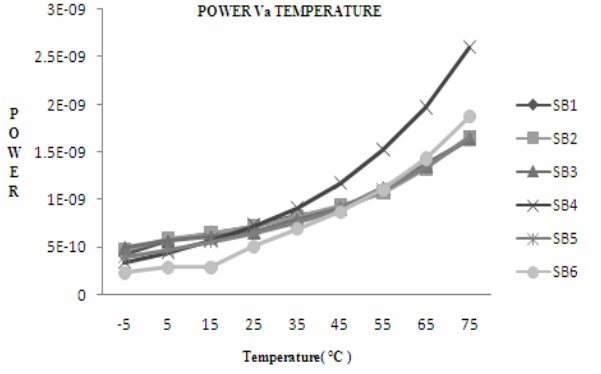

Fig. 7 Power Consumption Vs temperature at 45 nm technology

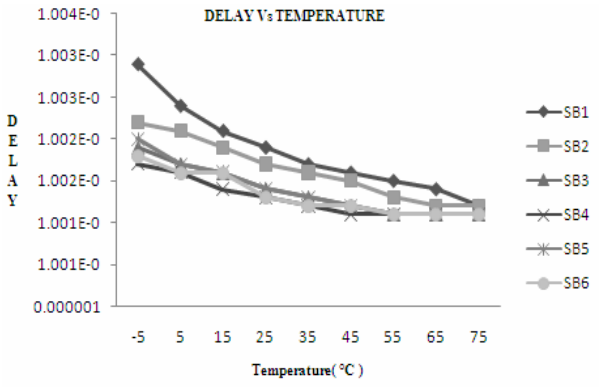

Fig. 8 Delay at various temperatures in 45 nm technology

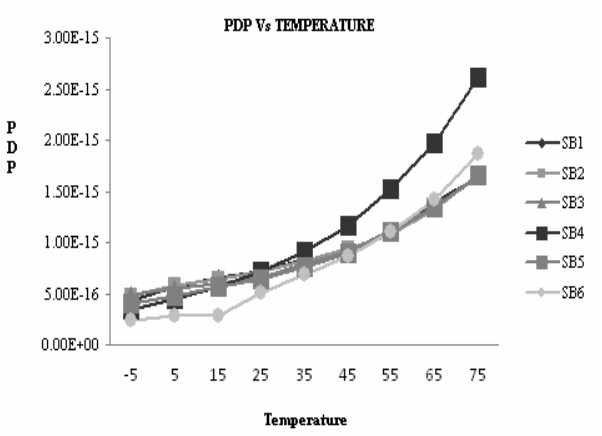

Fig. 9 Power-Delay Product Vs temperature at 45 nm technology

frequencies keeping the supply voltage at 0.22 V and temperature at 25°C in 45 nm technology. Fig. 3 - 4 show power consumption, Power Delay Product at different voltages with frequency of input signal 500 kHz and temperature of 25°C.

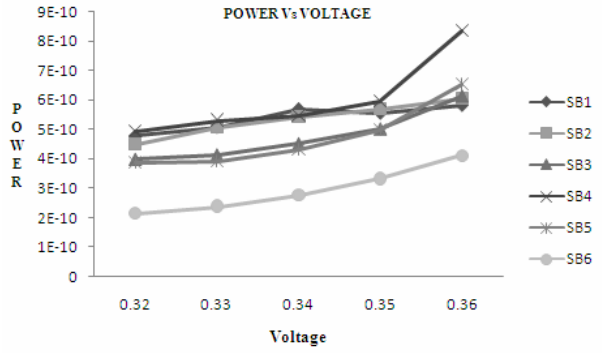

Fig. 10 Power Consumption Vs voltage at 65 nm technology

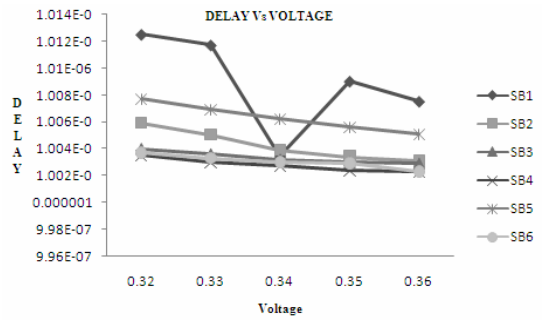

Fig. 11 Delay at different voltages in 65 nm technology

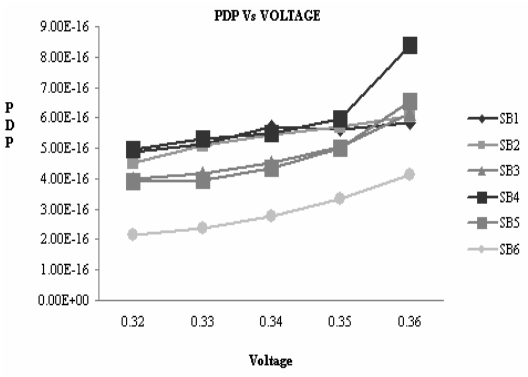

Fig. 12 Power-Delay Product at different voltages in 65 nm technology

Proposed SB6 biasing, in which the substrate of NMOS is connected to its source terminal and the substrate of PMOS is connected to clock condition, shows minimum power consumption, delay and Power delay product. At different frequencies with supply voltage of 0.22V and temperature of 25°C, SB6 biasing condition again shows minimum value of power consumption, and PDP (fig. 5 – 6). At 45 nm technology for different temperatures with input signal frequency of 500 kHz and voltage of 0.22V (fig. 7 – 9), SB6 consumes less power, introduces less delay and thus less power delay product.

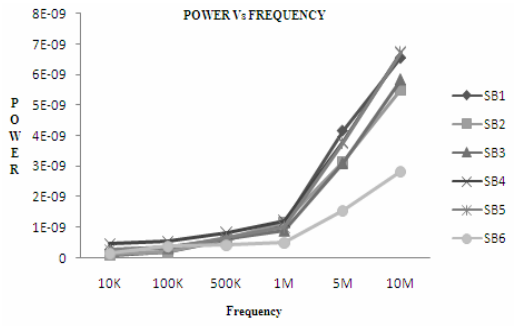

Fig.13 Power Consumption with frequency at 65 nm technology

Similar results are obtained in 65 nm technology confirming that the SB6 biasing is the best biasing for domino AND gate design. The power consumption by the gate is least at various supply voltages, when the SB6 biasing is used (fig. 10). The SB1 biased gate shows sudden decrease in delay at supply voltage of 0.34 V but at rest of the supply voltage it is showing the higher delay (fig. 11). SB5 biasing is showing least delay but overall power delay product is less in the proposed SB6 biasing (fig. 12). Though the power consumption with various biasing at various frequencies is almost equal (between 10 – 100 kHz) but as the frequency increases the power consumption by the gate with SB6 biasing is less than the other biasing schemes.

IV. CONCLUSION

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits. Techniques for domino circuits operating in the sub threshold region have been presented. Comparison of body bias methods using delay, power and PDP indicates that separately biasing the pre-charge and evaluation tree transistor bodies permits high-speed and energy-efficient ultra-low voltage domino circuits to be realized. Minimum energy in the sub threshold region then depends not only on supply voltage but also on the substrate bias voltage.

Simulation analysis reveals that the AND gate design using proposed SB6 biasing scheme is an energy efficient design.

REFERENCES

[1] V. Kursun and E. G. Friedman, "Low Swing Dual Threshold Voltage Domino Logic", *Proceedings of the ACM/SIGDA Great Lakes Symposium on VLSI*, April 2002.

[2] A. Alvandpour, P. Larsson-Edefors, and C. Svensson, "A Leakage Tolerant Multi-Phase Keeper for Wide Domino Circuits", *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems*, pp. 209-212, September 1999.

[3] S. Borkar, "Obeying moore's law beyond 0.18 micron", in Proc. IEEE Int. ASIC/SOC Conf., Sept. 2000, pp. 26–31.

[4] M. T. Bohr, "Nanotechnology goals and Challenges for electronic applications", *IEEE Trans.Nanotechnol.*, vol. 1, pp. 56–62, Mar. 2002.

[5] R. Ronen et al., "Coming challenges in microarchitecture and architecture", *Proc. IEEE*, vol. 89, pp. 325–339, Mar. 2001.

[6] M. W. Allam, M. H. Anis, and M. I. Elmasry, "High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies", *Proceedings of the IEEE International Symposium on Low Power Electronics and Design*, pp. 155- 160, July 2000.

[7] Narendra S., Tschanz J., Hofsheier J., Bloechel B., Vangal, S., Hoskote Y., Tang S., Somasekhar D., Keshavarzi A., Erraguntla V., Dermer G., Borkar N., Borkar S., De V., "Ultra-low voltage circuits and processor in 180nm to 90nm technologies with a swapped-body biasing technique", Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004, vol., no., pp. 156-518 Vol.1, 15-19 Feb. 2004.

[8] . Sharma, K. G. Sharma, B. P. Singh, N. Arora, "Efficient Interconnect Design with Novel Repeater Insertion for Low Power Applications," *World Scientific and Engineering Academy and Society (WSEAS) Transactions on Circuits and Systems*, Vol. 9, N0.3, pp. 153-162, March 2010.

[9] harma, Tripti Sharma, Prof.B.P.Singh, Manisha Sharma and Neha Arora, "Optimized Design of SET D Flip-Flop for Portable Applications", *International Journal of Recent Trends in Engineering and Technology*, vol. 4, no. 3, Nov. 2010.