A Novel Design for High Speed Multiplier for Digital Signal Processing Applications

(Ancient Indian Vedic mathematics approach)

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***Abstract*— In this paper, a high performance, high throughput and area efficient architecture of a multiplier for the Field Programmable Gate Array (FPGAs) is proposed. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on vertical and crosswise structure of Ancient Indian Vedic Mathematics. As per The proposed architecture, for two 8-bit numbers; the multiplier and multiplicand, each are grouped as 4-bit numbers so that it decomposes into 4×4 multiplication modules. It is also illustrated that the further hierarchical decomposition of 4×4 modules into 2×2 modules will not have a significant effect in improvement of the multiplier efficiency or in other words multiplier decomposition nearly reaches a saturation level in its efficiency at 4×4 decomposition. The coding is done in VHDL (Very High Speed Integrated Circuits Hardware Description Language) and the FPGA synthesis is done using Xilinx library.**

***Index Terms* — Vedic mathematics, vertically and crosswise algorithm, VHDL, Vedic multiplication.**

I. INTRODUCTION

With the latest advancement of VLSI technology the demand for portable and embedded Digital Signal Processing (DSP) systems has increased efficiently. Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. It is also the fastest growing technology this century and, therefore, it poses tremendous challenges to the engineering community. Faster additions and multiplications are of extreme importance in DSP for convolution, discrete Fourier transform, digital filters, etc. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them [6]. Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered, from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The whole of Vedic mathematics is based on 16 sutras. We discuss possible multiplier architecture of Vedic mathematics to be implemented on digital signal processing applications. A simple concept of digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. This method is complementary, direct and easy. In this paper, after a gentle introduction of urdhava triyakbhm Sutra, multiplier architecture is proposed and the architecture is illustrated with two 8-bit numbers; the multiplier and multiplicand, each are grouped as 4-bit numbers so that it decomposes into 4×4 multiplication modules. After decomposition, vertical and crosswise algorithm is applied to carry out the multiplication on first 4×4 multiply modules. The results of first 4×4 multiplication module are utilized after getting the sub product bits parallely from the subsequent module to generate the final 16-bit product. Hence any complex N×N multiplication can be efficiently implemented by using small 4×4 multiplier using the proposed architecture where N is a multiple of 4 such as 8, 12, 16, 20, 24…...4N. Therefore efficient multiplication algorithm implementation with small numbers such as 4-bits, can be easily extended and embedded for implementing efficient N×N multiply operation. This paper emphasizes that the further hierarchical decomposition of 4×4 modules into 2×2 modules will not have a significant effect in improvement of the multiplier efficiency n terms of area and speed.

II. VEDIC MATHEMATICS

We appreciate the efforts put by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics and also acknowledge the work of various people regarding Vedic Mathematics as the Vedic mathematics approach is totally different and considered very close to the way a human mind works. The multiplication of numbers is utilized in almost all branches of engineering; therefore the demand for high efficiency multiplier architecture increases. In this paper for the proposed digital multiplier we have used Urdhva-Tiryagbhyam sutra of Vedic mathematics. Vedic mathematics is based on sixteen sutras which serve as somewhat cryptic instructions for dealing with different mathematical problems [1]. Below is a list of those sixteen sutras, translated from Sanskrit into

English. And also there are some sub-sutras that are listed further.

- By one more than the one before
- All from 9 and the last from 10
- Vertically and crosswise
- Transpose and apply
- If the Samuccaya is the same it is zero
- If one is in ratio the other is zero
- By addition and by subtraction
- By the completion or non-completion
- Differential calculus
- By the deficiency
- Specific and general
- The remainders by the last digit
- The ultimate and twice the penultimate
- By one less than the one before
- The product of the sum
- All the multipliers

Below is a list of the Sub sutras or Corollaries:

- Proportionately.
- The remainder remains constant.
- The first by the first and the last by the last.
- For 7 the multiplicand is 143.
- By osculation.
- Lessen by the deficiency.
- Whatever the deficiency lessen by that amount and set up the square of the deficiency.
- Last Totaling 10.
- Only the last terms.• The sum of the products.
- By alternative elimination and retention.
- By mere observation.
- The product of the sum is the sum of the products.
- On the flag.

As In this paper we have used Urdhva-Tiryagbhyam sutra of Vedic mathematics. The comparison between the number of multiplication and addition required in the conventional and this method is shown in Table 1 [3] as follows.

TABLE 1 : COMPARISON BETWEEN NORMAL METHOD OF MULTIPLICATION AND VEDIC MATHEMATICS MULTIPLICATION

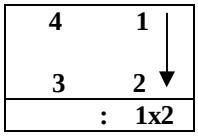
Normal method	Vedic method
For 2 bit multiplication Number of multiplications:4 Number of additions:2	For 2 bit multiplication Number of multiplications:4 Number of additions:1
For 3 bit multiplication Number of multiplications:9 Number of additions:7	For 3 bit multiplication Number of multiplications:9 Number of additions:5
For 4 bit multiplication Number of multiplications:16 Number of additions:15	For 4 bit multiplication Number of multiplications:16 Number of additions:9
For 8 bit multiplication Number of multiplications:64 Number of additions:77	For 8 bit multiplication Number of multiplications:64 Number of additions:53

A) Urdhva-Tiryagbhyam

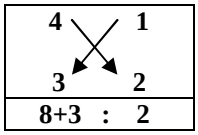
Urdhva-Tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It multiplies the numbers in the vertical and crosswise fashion so in English it is named as vertically and crosswise algorithm. We discuss multiplication of two and three digit numbers with this method as follows.

Multiplication of 2, two digit numbers as shown:

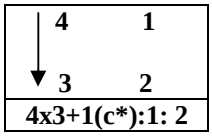
Step i)



Step ii)



Step iii)



This finally gives 1312

Let us work another problem by placing the carried over digits under the first row and proceed. But this time we will take 2, three digit numbers i.e. odd number of digits.

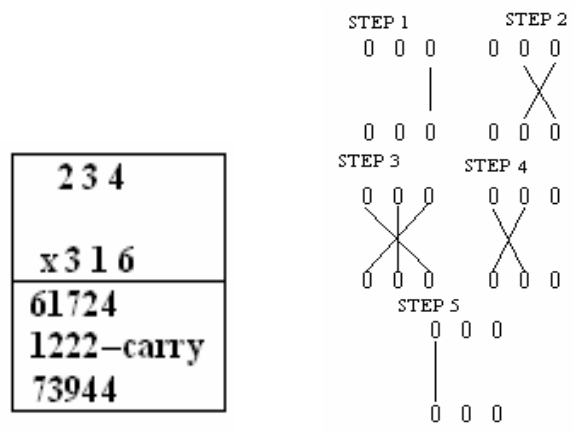


Figure 1: General rule for a 3 digit by 3 digit multiplication

Steps:

i) 4 X 6 = 24: 2, the carried over digit is placed below the second digit.

ii) (3 X 6) + (4 x 1) = 18 + 4 = 22; 2, the carried over digit is placed below third digit.

iii) (2 X 6) + (3 X 1) + (4 X 3) = 12 + 3 + 12 = 27; 2, the carried over digit is placed below fourth digit.

iv) (2 X 1) + (3 X 3) = 2 + 9 = 11; 1, the carried over digit is placed below fifth digit.

v) (2X3) =6.

vi) Respective digits are added.

The basic rule for the multiplication of two numbers of 4 digit is shown using the line drawing as follows.

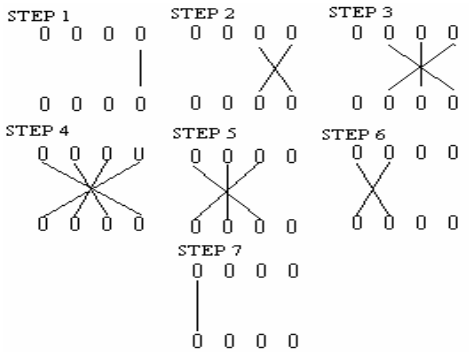


Figure 2: General rule for a 4 digit by 4 digit multiplication

The basic rule for the multiplication of two numbers of 6 digit is shown using the line drawing as follows. Similarly for any number of digits this multiplication technique of ancient Indian vedic mathematics can be used.

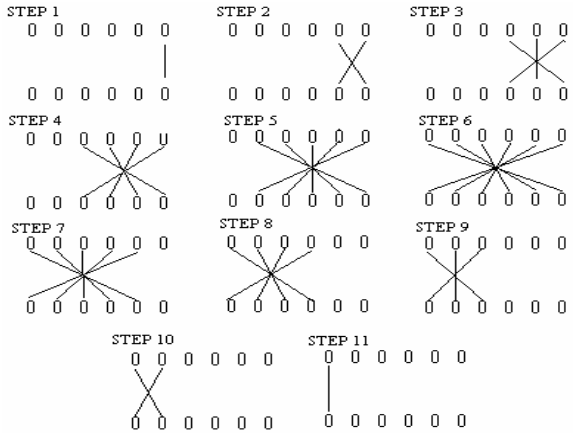


Figure 3 : General rule for a 6 digit by 6 digit multiplication

III. PROPOSED MULTIPLIER ARCHITECTURE

The conventional mathematics is an integral part of engineering education as most engineering system designs are based on various mathematical approaches. A multiplier is one of the key hardware blocks in most digital signal processing systems. With advances in technology, many researchers have tried to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. The hardware realization of the two bit number using the concept of the Urdhva-Tiryagbhyam sutra of the ancient Indian Vedic mathematics is shown in figure 4.

s1= (a0 and b0)
c1s2= (a1 and b0) + (a0 and b1)
s4s3= (a1 and b1)

Although it is found that the hardware realization for the two bit number using the conventional method of multiplication is same as that of the vedic multiplier.

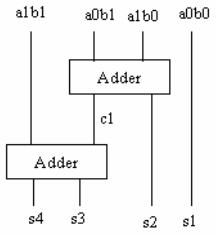
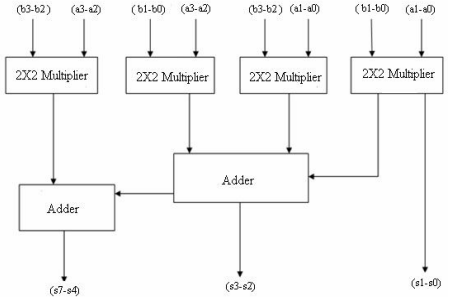


Figure 4 : Hardware realization of 2x2 bit multiplication

Similarly the hardware realization of the 2, four bit numbers, calling this realization of 2, two bit numbers can be made using the structural programming in the VHDL. The hardware realization of the 4x4 module according to the proposed multiplier is shown in figure 5.



RESULT = (s7- s4) & (s3- s2) & (s1-s0)

Figure 5 : Hardware realization of 4x4 bit multiplication

And similarly the basic building block of 8x8 bits Vedic multiplier is 4x4 bits multiplier which is implemented in its structural model. For bigger multiplier implementation like 8x8 bits multiplier the 4x4 bits multiplier units has been used as components which are implemented using Xilinx ISE8.2i library. The structural modeling of any design shows fastest design. The hardware realization of the 8x8 module according to the proposed multiplier is shown in figure 6.

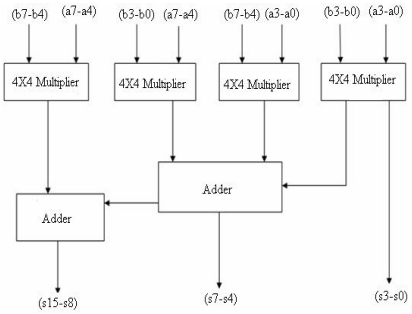
Now let the two numbers A and B of eight bit each and as per the proposed architecture they will be divided into two, four bit numbers to reduce the complexity and which will lead to high efficiency multiplier architecture.

A = a7 a6 a5 a4 a3 a2 a1 a0 (multiplicand)
B = b7 b6 b5 b4 b3 b2 b1 b0 (multiplier)

After these numbers are divided let the four bit numbers are d1, d0, e1, e0 where

A = a7 a6 a5 a4 | a3 a2 a1 a0
d1 | d0
B = b7 b6 b5 b4 | b3 b2 b1 b0
e1 | e0

D= d1d0= A= a7 a6 a5 a4 a3 a2 a1 a0
E= e1e0= B= b7 b6 b5 b4 b3 b2 b1 b0



RESULT = (s15- s8) & (s7- s4) & (s3-s0)

Figure 6 : Hardware realization of 8x8 bit multiplication

IV. MULTIPLIER IMPLEMENTATION

In this paper, the proposed multiplier architecture is implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language) and the FPGA synthesis is done using Xilinx ISE 8.2i. The design is optimized for speed and area using Xilinx, device family: Virtex XC4VLX15, package SF363, speed grade-12. The Xilinx Virtex XC4VLX15-12 device is to be applied and the device contains 6144 slices and 12288 input Look Up Tables and 240 bonded Input/output pads. Few multipliers have been designed using VHDL; Multipliers have been demonstrated for three different implementation styles and compared to prove that the further hierarchical decomposition of 4×4 modules into 2×2 modules will not have a significant effect in improvement of the multiplier efficiency n terms of area and speed. All are 8X8 multipliers based on Vedic mathematical method.

[a] The first implementation style is the Fully partitioned Vedic multiplier. Here for 8*8 multiplier implementation, 4x4bits multiplier units have been used as components; here each 2*2 bit sub-multiplication is done using Vedic multiplication, whose hardware realization is shown in figure 4, and 2*2bit sub-multiplication is used as components for 4*4 multiplier implementation, for 1 bit sub-multiplication, AND gate has been used.

[b] The second implementation style is the same as above ,accept that for two bits sub-multiplication the VHDL multiplication operator "*" is used.

[c] The third implementation style is most efficient style in terms of speed and area when compared to the above two methods. Here for 8*8 multiplier implementation, 4x4bits multiplier units have been used as components. And for four bits multiplication the VHDL multiplication operator "*" is used. The efficiency of this multiplier architecture proves that it is not efficient to decompose 4x4 modules into 2x2 sub-modules.

V. RESULT

The main point of this paper was to introduce a multiplier algorithm that is easy to learn and perform. The execution time of the three methods using Vedic multiplication algorithm are compared. It has been found that as the number of bit increases, hierarchical decomposition of 4×4 modules into 2×2 modules will not have a significant effect in improvement of the multiplier efficiency in terms of speed and area and there is a considerable improvement in the performance of the multiplier as proposed above in [c] as compared to [a] and [b]. The delays that follow are

TABLE II. COMPARISION BETWEEN THE EFICIENCY OF [A],[B],[C] IN TERMS OF SPEED AND AREA

	Path delay	Number of slices	Number of LUT's
[a]	10.893 ns	78 out of 6144	136 out of 12288
[b]	10.724 ns	81 out of 6144	143 out of 12288
[c]	10.441 ns	67 out of 6144	118 out of 12288

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