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Area Efficient High Speed FPGA Implementation of DUC for Ultrasonic NDE Signal Processing Techniques

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***Abstract*-In many Ultrasound Non Destructive Evaluation (NDE) [1] applications, the transducers are located far away from the evaluation site. Traditionally, low level analog signals are sent over long lines for instrumentation, which is prone to noise problems. In this project a different approach is followed by integrating digital signal processing functions in a single FPGA, to improve the information content of the output data stream. Digital Up Converter (DUC) is a digital circuit that implements the conversion of a complex digital baseband signal into a real passband signal and vice-versa. A DUC consists of a series of cascaded interpolation finite impulse response (FIR) filters, a mixer and a direct digital synthesizer (DDS). Typical design requirements shall include: (i) A relatively low sampling rate for the input complex base band signal, typically at digital modulation symbol rate. (ii) The baseband signal is filtered and converted to a higher sampling rate by modulating it to a direct digitally synthesized (DDS) carrier frequency. In this paper, these filters are designed using MATLAB [2] and Verilog HDL [3]. Functional verification is carried out using Xilinx ISE and the hardware implementation is done on Spartan 3E FPGA. The design issues explored in this paper include the optimization of DUC with respect to different parameters such as (i) The filters should be generic and programmable for a wide range of frequencies with good scalability (ii) The number of FIR interpolation Filter sections to be placed in cascade (iii) The required order of the filter (iv) The required sections of Cascaded Integrator Comb (CIC) Interpolation Filter[4] (v) Area efficient architecture and high speed implementation of the multiplier algorithm for the mixer [5], etc. The implemented DUC typically perform pulse shaping and modulation using an intermediate carrier frequency and make it extensively usable in NDE Signal Processing Techniques.**

***Keywords*: Digital Up Converter, FPGA, CIC Filter, Interpolation filters, NDE**

I. INTRODUCTION

A. Ultrasonic NDE

Non-Destructive Evaluation (NDE) [1] has found broad applications in the evaluation of product qualities, detection of flaws, etc., and ultrasonic NDE technique is the most widely used for its distinct features of broad spectrum of test objects. Ultrasonic NDE makes use of reflection and transmission properties of ultrasonic wave in materials to identify the location of defects. The operation process of ultrasonic NDE includes transmission of pulse, receiving of echoed signal, signal processing, and post-processing, among which signal processing is undoubtedly the most important stage, because it's in this stage that the received signals are denoised and analysed. Most ultrasonic inspection is done at frequencies between 0.1M and 25MHz.

The Digital up Converter is a digital circuit which implements the conversion of a complex digital baseband signal to a real passband signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically at the digital modulation symbol rate. The baseband signal is filtered and converted to a higher sampling rate before being modulated onto a direct digitally synthesized carrier frequency. The DUC typically performs pulse shaping and modulation of an intermediate carrier frequency. The input to the Digital Up Converter is an Ultrasonic signal ranging in frequency from 50k-1000 kHz.

The DUC consists of the following blocks

- Pulse shaping FIR filter
- Cascaded Integrator Comb (CIC) filter [4]
- Compensation FIR filter
- Direct Digital Synthesizer (DDS)
- Multiplier [5]
- Channel FIR filter [4]

II.ARCHITECTURE AND DESIGN IMPLEMENTATION

A. Description Of DUC

A block diagram of the Digital up Converter is shown in Figure 1.

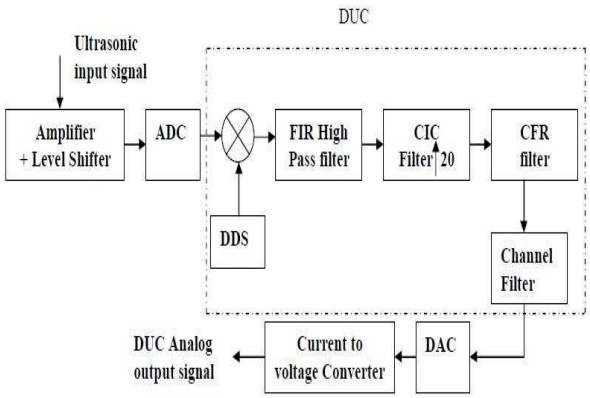


Figure 1. Digital Up Converter Block Diagram

The input to the Digital Up Converter is an Ultrasonic signal ranging in frequency from 50 KHz-1000 KHz. A 12 bit Analog-to-Digital (ADC) converter has the capacity of sampling signals up to the rate of 500 Ksps. The input Ultrasonic signal consists of frequency components that lie between 50 K- 1000 KHz. An optimum value of 256 KHz sampling frequency is chosen for the ADC. This 12 bit sampled composite digitized signal is fed to the multiplier in the DUC block and is configured in Spartan 3E FPGA.

The input signal is given to the multiplier wherein the signal is multiplied with 200 KHz fixed IF carrier generated by the DDS. The output generated from this DDS is 8-bit with a Spurious Free Dynamic Range (SFDR) of 60 dB. The 12-bit output from the multiplier is then filtered using a High-Pass Finite Impulse Response (FIR) filter to eliminate the lower sideband produced at the multiplier stage. A Cascaded Integrator-Comb filter up-samples the output of the FIR filter by a factor of 20 to attain a sampling rate of 5.12 MHz from 256 KHz. The output from the CIC filter is passed through a Channel Filter in order to take out the desired output signal (Upper Sideband). The resultant 5.12 MHz upsampled data is passed on to the DAC for converting the digital signal to analog form. The Digital-to-Analog (DAC) converter processes the 12-bit output from the channel filter. The DAC can handle maximum sampling rate of 125 Msps. Finally the modulated output is passed to a current to voltage converter (amplifier) for final transmission.

B. FIR FILTERS

Spectral shaping of the complex input signal is performed by the Pulse shaping FIR filter (PFIR) filter. The compensation finite impulse response (CFIR) filter and PFIR are polyphase multirate filter structures that interpolate by a factor of 2, 4 or 8. The filter length for each filter is configurable from 4 to 1024 taps. The coefficient precision can also be customized and ranges from 4 to 32 bits. In the typical interpolation filtering applications a reasonably flat pass band and narrow transition region filter performance is required. These desirable properties are not provided by the CIC filters alone, with their drooping pass band gains. Hence, the CFIR Filter is used to compensate for the droop in the passband of the CIC filter.

C. CIC Filter

Cascaded integrator-comb, also called Hogenauer filters [8], are multi-rate filters that are used for realizing large sample rate conversions in digital systems. The main advantage of this filter is that, it does not use multipliers, and consists of only adders, subtractors and registers [4]. They are typically employed in applications that have a large excess sample rate (the system sample rate is much larger than the bandwidth occupied by the signal).

CIC filters find application in

- Digital up converters and digital down converters.
- Channelization functions in a digital radio or MODEM
- For ultra-tight integration of GPS/INS/PL sensors
- Any filter structure that is required to efficiently effect a large sample rate change.

D. Characteristics of CIC Filter

Typical characteristics are

- Linear phase response;
- Utilize only delay and sum block (no multipliers);
- The integrator and comb structure need to be independent of rate changes (there is no need to reproject the filter on interpolation rate change).

E. CIC Interpolator

A CIC Interpolation filter has two major sections: a comb section, (a cascade of N combs) and an integrator section, (a cascade of N integrators). There is an interpolator or rate expansion switch (change by a factor R) between the two filter sections. The rate change switch is also known as a zero-stuffer as it pads zeros. The interpolator up samples the output of the last comb stage increasing the sample rate from fs/R to fs. One of the distinguishing factors of CIC filters is, the sampling rate of Comb filters is different from sampling rate of integrator, and the comb runs at a lower sampling frequency, which makes it easily programmable. Figure 2 gives a detailed structure of a CIC interpolator for 8 stages.

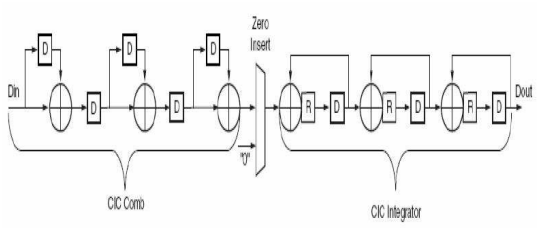


Figure 2. CIC Filter Structure Block Diagram

F. Comb

A comb filter running at a low sampling rate fs/R, for a rate change of R is an odd symmetric filter described by

$Y[n] = x[n]-x[n-RM]$ …….... (1)

In the equation, M is a design parameter and is known as differential delay. M is usually limited to 1 or 2. The corresponding transfer function at fs is

$Hc(z) = 1-z^{-RM}$ …… (2)

The comb sections are combined with a rate changer. Using a technique for multirate analysis of LTI systems the comb sections can be pushed through the rate changer and then become

$Y[n] = x[n]-x[n-M]$ …….. (3)

From the above equations the following are achieved:

1. Half of the filter has been slowed down and therefore efficiency is increased.
2. The number of delay elements required in the comb section had been reduced.
3. The integrator and comb stages are independent of rate changer.

The basic structure of a comb is as shown in figure 3.

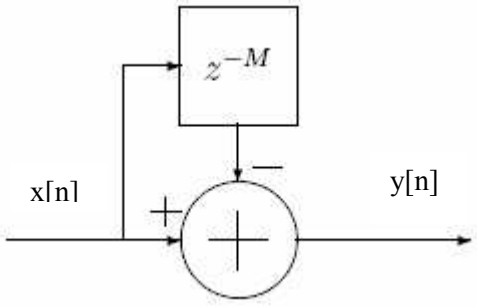


Figure 3. Basic Comb

G. Integrator

An integrator is a single pole IIR filter with a unity feedback coefficient given by

$Y[n] = y[n-1]+x[n]$ ……(4)

The transfer function for an integrator on the z-plane is

$H_I(z) = 1/(1-z^{-1})$ ……..…..(5)

The basic structure of an integrator is as shown in figure 4.

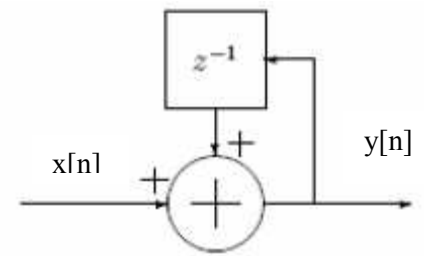
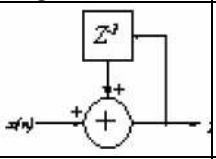
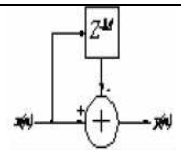


Figure 4. Basic Integrator

Table 1 shows the difference between Comb and Integrator stages in CIC filter derived in the above equations.

TABLE 1. Structure and Characteristics of Comb and Integrator

Items	Integrator	Comb
Structure		
Sampling Rate	f_s	f_s / R
y[n]	y[n-1] + x[n]	x[n] – x[n-RM]
$H_I(z)$	$\frac{1}{1-z^{-1}}$	$1-z^{-RM}$
$\lvert H(e^{j\omega}) \rvert$	$\frac{1}{2(1-\cos\omega)}$	$2(1-\cos RM\omega)$

H. Frequency Characteristics

The transfer function for a CIC filter at fs is

$H(z) = H_I^N(z)\, H_C^N(z)$ ……(6)

$H(z) = (1 - z^{-RM})^N / (1 - z^{-1})^N$……(7)

This equation shows that even though a CIC has integrators in it, which by themselves have an infinite impulse response, a CIC filter is equal to cascade of an N FIR filters, each having a rectangular impulse response with unit coefficients. The obtained frequency response of a CIC interpolator for an interpolation factor of 3 is as shown in figure 5.

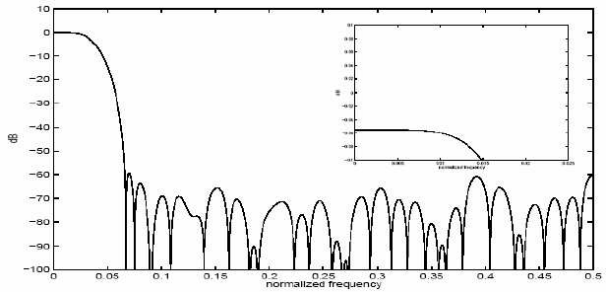


Figure 5. CIC Frequency Response

I. *Direct Digital Synthesizer*

A Direct Digital Synthesizer also known as Numerically Controlled oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It is an established method for generating periodic sinusoid signals, whenever high frequency resolution, fast changes in frequency, phase and high spectral purity of the output signal is required. A major advantage of the DDS is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly hop between frequencies.

J. *Theory of Operation*

A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The basic block diagram of a DDS is as shown in Figure 6.

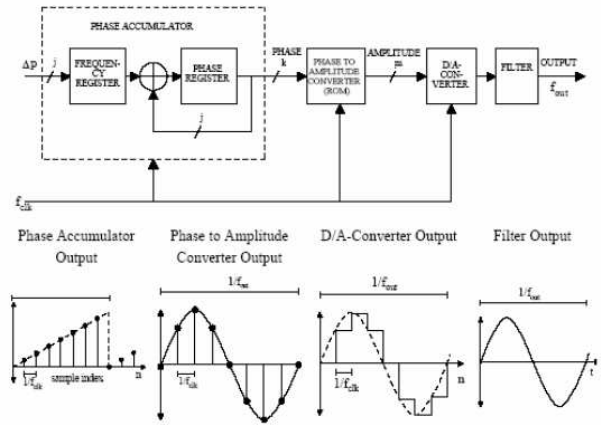


Figure 6. DDS Block Diagram with DAC and Filter

The implementation of the DDS can be divided into two distinct parts namely the phase accumulator (phase generator) and the phase to amplitude converter. The DDS can generate frequencies ranging from 50-1000 KHz with a resolution of 0.5 KHz and spurious free dynamic range (SFDR) of 60 dB. The 8-bit output data represents the generated sine wave.

K. *Multiply Accumulator*

MAC [5] is a parallel multiply-accumulator module. FIR filters typically are implemented in Xilinx FPGAs using either the MAC implementation or the DA (Distributed Arithmetic) technique. In DUC FIR filter implementation MAC based method is used. Figure 7 shows a MAC FIR filter simplified block diagram.

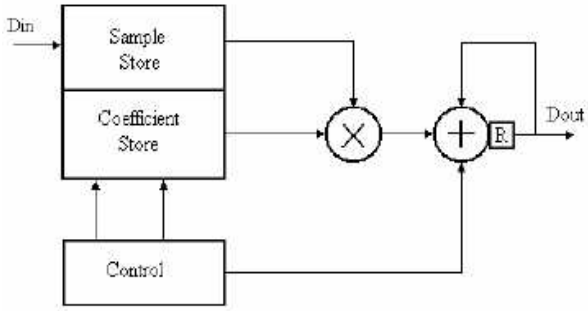


Figure 7. Simplified Block diagram of MAC

The MAC based architecture uses a multiplier to perform the tap product calculations, followed by an accumulator to perform the filter addition operations.

III. RESULTS AND DISCUSSIONS

DUC was developed in Verilog code [3] using Xilinx ISE tool. The code was simulated in ModelSim tool.

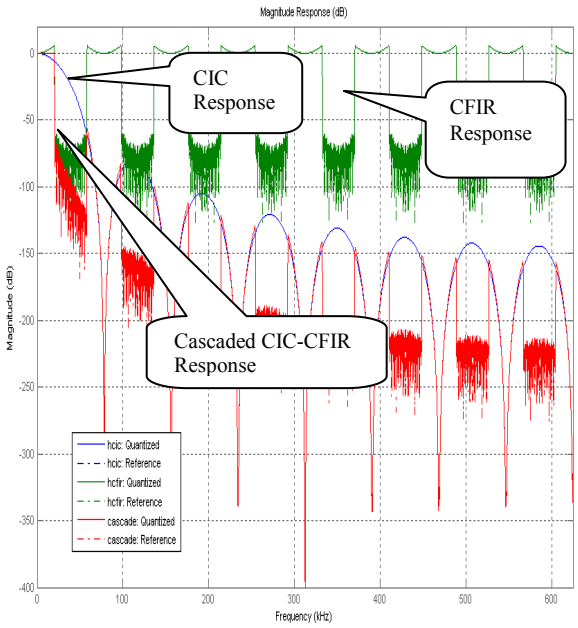


Figure 8. Working of the CIC-CFIR Filter and its Combined Response in MATLAB

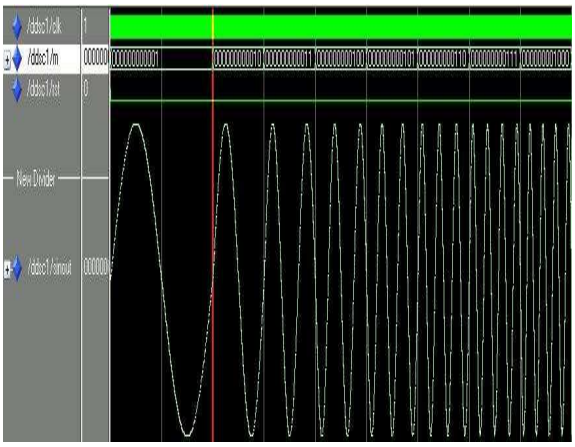


Figure 9. Simulation Results of DDS in MODELSIM

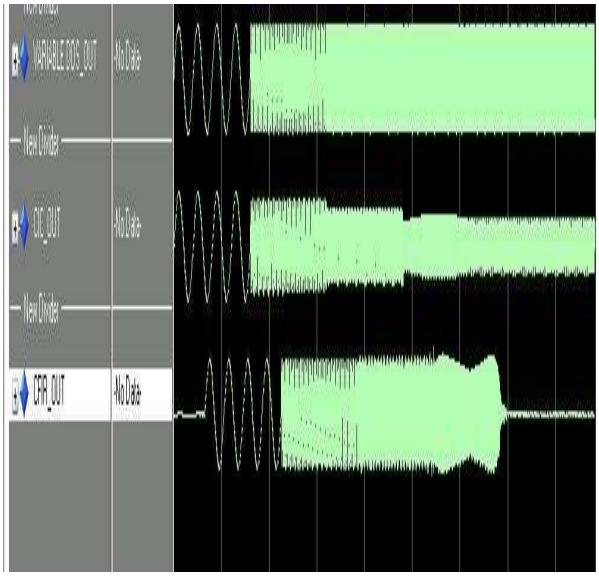


Figure 10. Simulated output of DDS, CIC filter, CFR FIR filter

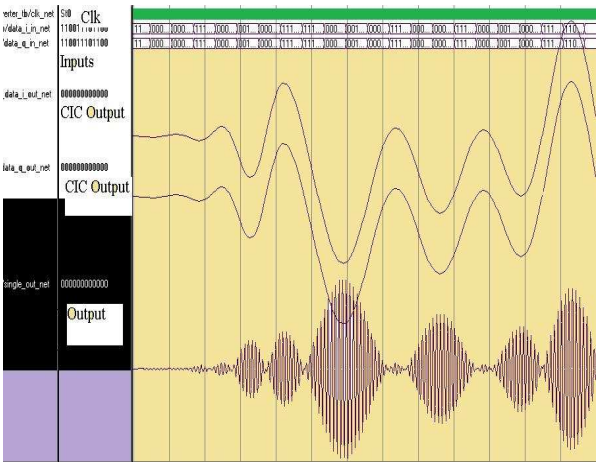


Figure 11. Simulation of Digital Up Converter

The device utilization summary is listed in Table 2.

Table 2. Device utilization summary of Spartan 3E FPGA

Device Utilization Summary:

Selected Device : 3s500epq208-5

Number of Slices:	1104	out of 4656	23%
Number of Slice Flip Flops:	850	out of 9312	9%
Number of 4 input LUTs:	3428	out of 9312	36%
Number used as logic:	1812		
Number used as RAMs:	1616		
Number of IOs:	111		
Number of bonded IOBs:	83	out of 158	52%
IOB Flip Flops:	13		
Number of MULT18X18SIOs:	6	out of 20	30%
Number of GCLKs:	7	out of 24	29%
Number of DCMs:	1	out of 4	25%

Timing Summary:

Speed Grade: -5
Minimum period: 31.402ns (Max Freq: 31.845MHz)
Minimum input arrival time before clock: 7.497ns
Maximum output required time after clock: 15.523ns
Maximum combinational path delay: 17.713ns

From the above results, the verilog code for DUC is optimized to achieve less area and high speed of operation.

IV. CONCLUSIONS

This paper deals with the development of a DUC for NDE Signal processing applications. The base band signal that is received by the equipment is in the range of 50 KHz – 1000 KHz. The carrier signal frequency that is used to modulate the signal lies between 100 KHz – 1000KHz. DUC block was developed to modulate the message signal. In this design the interpolation filters were cascaded along with a DDS and a mixer to get the required output. Coding of the sub-blocks of DUC has been implemented using Verilog. Simulations were carried out for the coded blocks and the results have been verified using ModelSim. The Verilog code is synthesized using Xilinx ISE and the coefficients for the interpolation filters were verified using MATLAB. Synthesized Verilog code is implemented using Spartan 3E XC3S500E-5PQ208 that has 158 user IO's.

V. REFERENCES

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